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26304 7590 04/12/2010 KATTEN MUCHIN ROSENMAN LLP 575 MADISON AVENUE NEW YORK, NY 10022-2585			EXAMINER ARCOS, CAROLINE H	
			ART UNIT 2195	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/733,174	Applicant(s) OKA ET AL.	
	Examiner CAROLINE ARCOS	Art Unit 2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 January 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-11 are pending for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-11 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- a. The following terms lacks antecedent basis:
 - i. The entire processing - claim 1 and claim 7.
- b. The claim language in the following claims is not clearly understood:
 - i. As per claim 1, line 4, it is unclear what is meant “operating environments” (e.g. mode or different operating system). Line 7, it is unclear how the configuration of the environment is done (e.g. activate the processor). it is unclear whether multiple operating environments is configured for each selected processor at one time (multiple operating environment active at one on each processor) or configure one operating environment at a time. Line 8, it is unclear what does “entire processing” represent (e.g. whole system load)
 - ii. As per claim 7, line 9, it is unclear whether each component processor operates in a plurality of environment at once or change operating environment one at a time. Line 15, it is not clearly understood what is meant

by "configure the operating environment" (e.g. activate the processor) and what is meant by "operating environment" (i.e. operating system or mode of operation: serial or parallel).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Rawson, III (US 2003/0115495 A1) and further in view of Jeddeloh et al. (US 5,414,857).

5. As per claim 1, Branco teaches the invention substantially including a signal processing device, comprising:

a general-purpose signal processor of plurality of component- processors, each of the component-processor is capable of operating under a plurality of operating environments associated with a plurality of software tasks and operating independently from other component - processor (abs., lines 1-16; col. 1, lines 3-41; col. 3, lines 42-col.4, lines 16);

a management processor for configuring the operating environment of each of the selected component- processors (col. 3, lines 42-col.4, lines 16).

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6. Branco does not explicitly teach a management processor for selecting a number of component- processor to operate and for configuring the operating environment of each of the selected component- processors in response to a type of processing and an estimate load of an entire processing.

7. However, Rawson teach selecting a number of component- processor to operate in response to an estimate load of an entire processing (abs., lines 1-18; par. [0007]; par. [0017]; par. [0018]; claim 17).

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco and Rawson because Rawson teaching of estimating the workload and determines based on the estimation a number of component- processors to operate would benefit the system performance, improve system resource usage and increase power saving.

9. The combined teaching of Branco and Rawson does not explicitly teach that the management processor for configuring the operating environment of each of the selected component- processors in response to a type of processing.

10. However, Jeddelloh teaches the management processor for configuring the operating environment of each of the selected component- processors in response to a type of processing (abs.; col. 1, lines 45-65; col. 2, lines 17-20; col. 2, lines 65-col. 3, lines 2; col. 4, lines 20-40;

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col. 8, lines 15-36).

11. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Rawson and Jeddelloh because Jeddelloh teaching of configuring the environment of each of the selected component- processors in response to a type of processing would control the system based on the type of processing.

12. As per claim 2, Branco teaches an input/output interface for receiving a signal to be processed inputted from an external device or one of the component-processors (col. 1, lines 45-67; col. 2, lines 1-15; col. 5, lines 37-67) and wherein the management processor controls the input/output interface to swap one of the component-processors which receives the signal to be processed which is inputted through the input/output interface or outputs the processed signal in accordance with a demand for signal processing (col. 1, lines 50-55; col. 3, lines 43-67).

13. As per claim 5, Branco teaches a local memory is disposed on each of the component-processors, said local memory stores a signal to be processed or a signal processed result by the component-processors until the signal to be processed or the signal processed result becomes available to be outputted to the input/output interface (col. 1, lines 46, lines 49; col. 2, lines 35-38).

14. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Rawson, III (US 2003/0115495 A1), and further in view of Jeddelloh et

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al. (US 5,414,857) as applied to claim 2 above and further in view of Macias et al. (US 5,886,537).

15. As per claim 3, the combined teaching of Branco, Rawson and Jeddelloh does not explicitly teach the input/output interface includes a cross bus switch that can selectively connect the external device to one of the component-processors, or the component-processors to each other.

16. However, Macias teaches the input/output interface includes a cross bus switch that can selectively connect, under the control of the management processor, the external device to one of the component-processors, or the component-processors to each other (Fig. 1).

17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Branco, Rawson Jeddelloh and Macias because Macias teaching of a cross bus switch that can connect the component-processors to each other would allow easier communication between different processor in the system.

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Rawson, III (US 2003/0115495 A1) and further in view of Jeddelloh et al. (US 5,414,857) as applied to claim 2 above and further in view of Iwase et al. (US 5,926,583).

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19. As per claim 4, the combined teaching of Branco, Rawson and Jeddeloh doesn't explicitly teach the input/output interface includes a multiple bus that can connect the component-processors to each other.

20. However, Iwase teaches the input/output interface includes a multiple bus that can connect the component-processors to each other (col. 31, lines 18-45).

21. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Rawson, Jeddeloh and Iwase because Iwase teaching would regulate communication efficiently between different components of the system.

22. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Rawson, III (US 2003/0115495 A1), and further in view of Jeddeloh et al. (US 5,414,857) as applied to claim 2 above and further in view of Arnold et al. (US 5,175,837).

23. Claim 6, the combined teaching of Branco, Rawson and Jeddeloh does not explicitly teach the general-purpose signal processor, the management processor and the input/output interface are disposed in a single case, the case including a first connection interface being connectable to a device that provides a demand for signal processing to the management processor, and a second connection interface being connectable to the external device that delivers a signal with respect to the input/output interface.

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24. However, Arnold teaches the case including a first connection interface being connectable to a device that provides a demand for signal processing to the management processor, and a second connection interface being connectable to the external device that delivers a signal with respect to the input/output interface (Fig. 1, element 18, 20A).

25. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Rawson, Jeddelloh and Arnold because Arnold teaching would facilitate the communication between different components of the system.

26. The combined teaching of Branco, Rawson, Jeddelloh and Arnold does not explicitly teach that the general-purpose signal processor, the management processor and the input/output interface are disposed in a single case. However, it is well known to one of ordinary skill in the art at the time the invention was made to conclude that all three components are disposed on a single case for portability.

27. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Macias et al. (US 5,886,537), in view of Rawson, III (US 2003/0115495 A1) and further in view of Jeddelloh et al. (US 5,414,857).

28. As per claim 7, Branco teaches an entertainment device, comprising:
a signal processing device including a general-purpose signal processor (abs.,

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lines 1-13; col. 1, lines 44-67; col. 2, lines 1-67)

a management processor (col. 3, lines 43-67; col. 4, lines 1-12) and an input/output interface (col. 1, lines 50-55; col. 2, lines 39-45); and

the general-purpose signal processor is formed of a plurality of component-processors, each of the component-processors operates in parallel under a plurality of operating environments associated with software tasks and independently from other component-processors(abs.; col. 1, lines 37-67; col. 2, lines 1-67; col. 3, lines 42-col.4, lines 16);

wherein the management processor configures the operating environments for each of the component-processors in accordance with a demand for signal processing (col. 3, lines 43-67; col. 4, lines 1-12);

the input/output interface so as to swap one of the component-processors which receives the signal to be processed which is inputted through the input/output interface or outputs the processed signal in accordance with the demand for signal processing(col. 1, lines 50-55; col. 2, lines 39-45).

29. Branco does not explicitly teach a main processor that provides a demand for signal processing to the signal processing device, the input/output interface inputs a signal to be processed from an external device or one of the component-processors, and outputs a processed signal to the external device or one of the component-processors, and the management processor select a number of component-processor to operate in response to a demand for signal processing, wherein the demand for signal processing is estimated based on a

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type of processing and estimated load of the entire processing

30. However Macias teaches the input/output interface inputs a signal to be processed from an external device or one of the component-processors, and outputs a processed signal to the external device or one of the component-processors (col. 3, lines 31-67; col. 4, lines 1-3; Fig. 1).

31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco and Macias because Macias teaching of input/output interface inputs a signal to be processed from an external device or one of the component-processors, and outputs a processed signal to the external device or one of the component-processors would be known to one of ordinary skill in the art as one of the function of input/output interface which facilitate the communication between different components of the system.

32. The combined teaching of Branco and Macias does not explicitly teach wherein the management processor estimates an entire load of processing, and determines based on the estimation a number of component-processors to operate.

33. However, Rawson teaches the management processor select a number of component-processor to operate in response to a demand for signal processing, wherein the demand for signal processing is estimated load of the entire processing (abs., lines 1-18; par. [0007]; par.

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[0017]; par. [0018]; claim 17).

34. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco and Rawson because Rawson teaching of estimating the workload and determines based on the estimation a number of component-processors to operate would benefit the system performance, improve system resource usage and increase power saving.

35. The combined teaching of Branco, Macias and Rawson does not explicitly teach that a main processor that provides a demand for signal processing to the signal processing device and wherein the demand for signal processing is estimated based on a type of processing.

36. However, Jeddeloh teaches a demand for signal processing to the signal processing device and wherein the demand for signal processing is estimated based on a type of processing. (abs.; col. 1, lines 45-65; col. 2, lines 17-20; col. 2, lines 65-col. 3, lines 2; col. 4, lines 20-40; col. 8, lines 15-36).

37. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Rawson and Jeddeloh because Jeddeloh teaching of configuring the environment of each of the selected component-processors in response to a type of processing would control the system based on the type of processing.

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38. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Macias et al. (US 5,886,537), in view of Rawson, III (US 2003/0115495 A1) and further in view of Jeddeloh et al. (US 5,414,857) as applied to claim 7 and further in view of Takeda et al. (US 2002/0068626 A1).

39. As per claim 8, the combined teaching of Branco, Macias, Rawson and Jeddeloh does not explicitly teach a network interface that enables a connection with a computer network, and a storage means that stores digital information readable by a computer, wherein the main processor controls the network interface to acquire the digital information from an external device, stores the acquired digital information in the storage means, and provides the stored digital information and a demand for signal processing based on the digital information to the management processor of the signal processing device to constitute operating environments for entertainment processing the contents of which are determined in accordance with the digital information.

40. However, Takeda teaches a network interface that enables a connection with a computer network, and a storage means that stores digital information readable by a computer, wherein the main processor controls the network interface to acquire the digital information from an external device, stores the acquired digital information in the storage means, and provides the stored digital information and a demand for signal processing based on the digital information to the management processor of the signal processing device to constitute operating environments for entertainment processing the contents of which are determined in accordance with the digital information (Fig. 1; fig. 2; par. [0033]; par. [0035]; par. [0045]; par. [0046]; par. [0047]; par.

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[0052]).

41. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Macias, Rawson, Jeddeloh and Takeda because Takeda teaching would elaborate on Branco teaching of command external to the controller which control and generate the demand for signal which is well know to one of ordinary skill in the art to have a master or main processor regulating the demand for the signal and slave processors performing the tasks.

42. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Macias et al. (US 5,886,537), in view of Rawson, Ill (US 2003/0115495 A1), in view of Jeddeloh et al. (US 5,414,857) and in view of Takeda et al. (US 2002/0068626 A1) as applied to claim 8 above, further in view of McNeil et al. (US 4,876,643).

43. As per claim 9, Branco teaches that through the management processor, the operating environments is constructed for processing on one or more of the component- processors through the management processor, and, after constructing the operating environments, reconstructs said operating environments to new operating environments upon receipt of another digital information which differs from said digital information (col. 3, lines 43-67; col. 4, lines 1-16).

44. The combined teaching of Branco, Macias, Rawson, Jeddeloh and Takeda does not explicitly teach that the constructing and reconstructing is done by the main processor. However,

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McNeill teaches that the constructing and reconstructing is done by the main processor (col. 3, lines 50-60; col. 4, lines 35-53).

45. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Macias, Rawson, Jeddelloh and McNeil because McNeil teaching would elaborate on Branco teaching of command external to the controller which control and generate the demand for signal which is well know to one of ordinary skill in the art to have a master or main processor regulating the demand for the signal and slave processors performing the tasks.

46. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Macias et al. (US 5,886,537), in view of Rawson, III (US 2003/0115495 A1) in view of Jeddelloh et al. (US 5,414,857) and further in view of Takeda et al. (US 2002/0068626 A1) as applied to claim 8 above, and further in view of Gorgone et al. (US 2003/0200249 A1).

47. As per claim 10, the combined teaching of Branco, Macias, Rawson, Jeddelloh and Takeda does not explicitly teach the digital information comprises plural kinds of application programs that can execute required functions, respectively, and wherein the management processor assigns any of the functions to the corresponding component-processors, and reads a corresponding application program for executing the assigned function from the storage means,

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and executes the application program.

48. However, Gorgone teaches plural kinds of application programs that can execute required functions, respectively, and wherein the management processor assigns any of the functions to the corresponding component-processors, and reads a corresponding application program for executing the assigned function from the storage means, and executes the application program (Par. [0016]).

49. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Macias, Rawson, Jeddeloh, Takeda and Gorgone because Gorgone teaching of processing plurality of application kinds with different function would improve the performance and efficiency and the diversity of processing application and increase the throughput.

50. As per claim 11, McNeill teaches that each of the component-processors operates only for executing the application program for executing the function assigned to the component-processor until the management processor provides another demand to the component-processor (abs., lines 3-9; col. 3, lines 50-60).

Response to Arguments

51. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

52. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

53. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151.

The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

54. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Caroline Arcos/
Examiner, Art Unit 2195

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